PhD RESEARCH FINDINGS

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PhD Topic: "**Design and Simulation of High Performance III-V Compound Based Semiconductor Devices**"

PhD Research Findings:

This thesis is centred around designing and investigating III-V homogeneous and heterogeneous TFET, which can enable V_{DD} reduction without compromising the ON-state performance, and keep the Moore's law valid and alive. The 2D-TCAD simulation methodology has been used for the design and investigation at device and circuit level. The finding of the research has been briefly summarized in the following points.

- Si/GaAs TFET can significantly outperform the conventional Si TFET in terms of ambipolarity suppression, ON current, OFF current and gate capacitance, and it can provide better performance at both the circuit and device level.

- Replacing uniform doping in TFET with lateral gaussian doping can provide much improved TFET performance ON state, however, at lower channel length gaussian doping decay need to be sharp.

- Pseudo-split gate InGaAs TFET can provide much better suppression of ambipolar current than Overlapping gate-on-drain TFET, along with much reduced parasitic capacitance.

- III-V TFET are more sensitive to ITCs because of absence of native oxide and lower effective mass. The impact of both main gate ITCs and back-side ITCs has been investigated in InGaAs TFET, and it has been observed that back-side ITCs significantly alter the device characteristics. A design level measure has been proposed to mitigate this impact.

- Although low bandgap III-V TFET can provide much better ON-state performance than Si TFET and seems to be future alternative to MOSFETs, but they are more sensitive to ITCs and structural and material parameter variation. Further, they generally exhibit higher leakage, hence they need to be designed carefully so as not to override their benefits with their limitation.