Ph.D. RESEARCH FINDINGS

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Ph.D. Topic: "**DESIGN AND SIMULATION OF HIGH PERFORMANCE EMERGING NANOELECTRONIC DEVICES**"

Ph.D. Research Findings:

This thesis work focuses on the design and development of high performance low-power nanoelectronic transistors. It aims to address the several issues in nanoscale transistors by providing solutions to suppress the OFF-state parasitic current component, improved ON-OFF current ratio, abrupt source-channel junction requirement, etc., for both the JL FET as well as the TFET devices. Extensive 2-D TCAD simulations have been carried out for analyzing new device structures. The research findings have been briefly summarized below:

- A novel structure of an n-channel SOI JLT is proposed, termed as buried-metal n-SOI JLT. The device employs a buried-metal-layer to improve the device characteristics which helps in suppressing the parasitic leakage along with the SCEs in a conventional single-gate n-SOI JLT. The depletion region formed at the bottom of the device layer due to Schottky junction helps in achieving the volume depletion in the OFF-state.

- To improve TFET driving capacity, a point TFET incorporating the concept of vertical-gaussian doping in an ultra-thin device layer is introduced. Along with this, the source region is realized via ED concept. The device improves the BTBT at the source-channel junction and consequently, much improved DC and analog performance is observed compared to the conventional TFET.

- As research shifted from point to line tunneling device structures, a dual MOSCAP based vertically elevated channel-drain line TFET is proposed. The simulation study shows that it has improved electrostatic integrity, suppresses leakage in the subthreshold region, and has better drive current.

- The potential of low band gap and high mobility III-V material system in a TFET design is also harnessed. Based on a stepped broken-gap band alignment alongside ED regions, a TFET for ultra-low power is proposed and simulated. The device design aspects and the transient characteristics are also studied.

- Instead of a conventional method of improving a single device unit to improve its performance, an alternative method of increasing the functionality per unit device is also proposed. A reconfigurable FET that can be programmed dynamically by external voltage is introduced. The re-engineered silicide drain allows for the complementary switching operation. A complete inverter operation can also be realized at the device level of encapsulation