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Topic: Modeling and Simulation of Novel Nanoelectronic Devices based on Silicon on Insulator technology

Abstract

The overwhelming evolution of electronics, information technology (IT), and communications has been mainly attributed by continuous scaling of silicon-based complementary metal-oxide-semiconductor (CMOS) technology. Silicon based devices has continued until today and has reached to the nanoscale (<32 nm) range. Because of the incredible advantages of the silicon over the other semiconductor materials, more than 90% devices are made up of silicon. The ever increasing demands for improved performance in terms of speed, area, and power dissipation have forced the scientists/engineers to scale down the devices further and further in order to keep Moore's law alive. We have already entered in the terascale regime. ***The technologists working in the field of nanoelectronics would like visionaries to address two key questions: How long will the silicon CMOS technology will remain in the market? And what will happen after it?*** Most of the researchers working in the field of nanoelectronics believe that Moore's law is already saturated and it is not possible to continue with silicon based MOSFETs. The various issues, like short channel effect, increase in leakage, mobility degradation, oxide tunneling, channel transport limitations, doping related issue, and increase in source/drain series resistance etc. that becomes big obstacle below 32/22 nm technology node. Besides this scaling needs to scale supply voltage, in order to keep electric field well below the critical field, in order to operate device properly.

Therefore electronics and IT is currently in an immediate need of the devices or materials, which can replace silicon, based MOSFET and extend Moore's law further. However, the new devices must possess clear advantages to their conventional counterpart. Many new devices based on new physics and new materials have been explored to enhance scaling below 10nm technology node. Many novel devices are currently there, like Tunnel FET, Schottky Barrier MOSFET (SB-MOSFET) FinFET, double gate MOSFET, Pi-FET, Gamma FET; however, it appears extremely difficult to replace the conventional bulk MOSFET by these alternative devices. These types of device either have complex device geometry or have poor performance in comparsion to conventional MOSFET.

Besides this nanoscaled devices are greatly hindered by doping related issues. The dopingless/charge plasma based devices are currently in interest of researchers to mitigate the doping related issues at the nano level. These types of devices don't require conventional technique for doping the necessary regions, as these regions are created by different metal work-function engineering. So such devices are free from doping related issues and can fabricated at low temperature.

Study area: Semiconductor devices, Charge plasma, Doping-less, BJT, MOSFET.

Objectives:

The ultimate objective of this thesis was to develop a new and novel SOI-based technology to enhance the scalability of MOS devices in the nanometer range. The major issues of Random dopant fluctuations, self heating effects and short channel effects in SOI-based MOS devices, which act as a significant hurdle in the further scaling of the devices, has been tackled. By Addressed these problems

have increase the scalable properties of SOI MOSFETs, and MOS devices with feature sizes less than 10 nm. Further, it will have a significant impact on the scope, performance and overall reliability of the devices. The Moore's law will remain valid for some more time without making shift from silicon technology to other costlier devices technologies, such as carbon nanotube (CNT), Graphene, Gallium Nitride (GaN) etc. materials based devices devices.

Software Used: *ATLAS* Device Simulation Software. SILVACO, Inc. 4701 Patrick Henry Drive, Bldg. Santa Clara, CA 95054 Telephone (408) 567-1000, Internet: www.silvaco.com

Summary and Conclusion

In this work a simulation study of Charge plasma based lateral bipolar junction transistor, Tunnel FET and Schottky barrier MOSFET is carried out for their possible application in mixed signal technology, BiCMOS realization and power electronics. An extensive simulation study of the key thermal and electrical characteristics of both types of devices have been rigorously performed using ATLAS/ATHENA (Silvaco) device and process simulators. The main issues addressed in the TFET and SB-MOSFET device are low ON current and the short channel effects. Similarly, in the lateral bipolar transistor on SOI, it is the problems of low current gain, breakdown voltage, on-resistance and the self-heating which have been addressed. Some new and novel device structures have been proposed and analyzed in both categories of devices to alleviate the above mentioned issues. The state-of-the-art work related to this thesis, important observations and results from the simulation study have been organized in the first seven chapters of this thesis, followed by conclusion and future work in this chapter.

The chapter 1 is an introductory chapter, mainly gives the motivation behind this work. The chapter 2 presents the state-of-the-art work or literature survey related to charge plasma based SOI devices and lateral bipolar transistors on SOI.

In chapter 3 and chapter 4, extensive simulation studies of SELBOX based BCPT and *p* type BCPT have been performed. In chapter 3, a comparative analysis of various characteristics of Conventional SOI BJT, BCPT and the SELBOX BCPT devices have been performed.

The charge plasma concept has been applied to *p* type BJT in chapter 4. A novel high performance PN Schottky collector lateral junction transistor (BJT) on silicon-on-insulator (SOI) has been proposed. The proposed device addresses the problem of poor speed of conventional lateral PNP-BJT device by using a Schottky collector.

In chapter 5, the problem of ON current in conventional charge plasma and doped TFET have been addressed. A novel structure of gate engineered TFET has been proposed. The device results in higher ON current, higher transconductance, higher ON OFF ratio, higher cutoff frequency and lower delay at circuit level in comparsion to conventional charge plasma and doped TFET.

In chapter 6, we address the problem low ON current and the fabrication complexity faced by conventional SB-MOSFET and DSL-SB-MOSFET respectively. We proposed and simulation study of a source engineered SB-MOSFET. The use of dual source metal work-function at the source side is the novelty of the device. Erbium silicide (ErSi1.7) is used as the main source material, and Hafnium is used as a source extension. The use of Hafnium as a source extension induces an n+-type charge plasma in an undoped silicon film, which significantly improves the performance of the proposed device.