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ABSTRACT

The widespread applications of fuzzy logic in various fields have been hindered by the problem of low speed of operation of fuzzy processors. Both hardware and software approaches have been adopted to increase the speed of operation of the fuzzy processors in general and inference processing in particular. However, the software based approach is the slowest among all. The low speed is fuzzy processors is generally contributed by the inference engine of a fuzzy processor, which demands high latency for calculating the matching degree (MD) between the fuzzified input and the antecedent membership functions.

The main objective of this work is to design and implement fuzzy inference processors with emphasis on enhancement of processing speed, power consumption reduction and flexibility. Novel architectures of fuzzy inference processors have been proposed and implemented in field programmable gate array (FPGA). The architectures developed are power, area and speed efficient. An important part of fuzzy processing system is fuzzy inferencing, which is being used to build an efficient human expert system. The performance of the fuzzy inferencing system has a strong impact on the overall performance of the fuzzy processor. The processing speed of inference engine is an important issue and has been addressed in this work. The speed bottleneck of the inference engine lies in the calculation of the matching degree (MD) between the fuzzified input and the antecedent membership functions (MF). Generally, the problem with MD calculation is that it needs very high latency, which actually limits the overall performance of the fuzzy system. In this work, we addressed the inference processor speed problem by proposing novel architectures of MAX-MIN calculator circuit for calculating the matching degree. Initially in this work three types of MAX-MIN calculator circuits have been designed and accordingly three complete fuzzy inference processors based on these MAX-MIN calculators have been designed and implemented. The three MAX-MIN calculators calculate the MD between the three types of MFs, such as, triangular, trapezoid and

Gaussian shaped fuzzified input and the antecedent MFs. Besides the above mentioned three fuzzy inference processors, a fourth novel fuzzy inference processor based on multi membership function (MMF) has been designed and implemented first time to our knowledge. The MMF based fuzzy inference processor is handling three MFs, Gaussian, trapezoid and triangular MFs together. All the designed architectures are power, area and speed efficient in comparison to existing architectures, as they generally consume less multiplexing and subtracting operations in comparison to existing architectures. Further, in each and every proposed fuzzy processor, all the blocks like fuzzifiers, inference engine, fuzzy decoders and defuzzifiers have been modelled in very high speed hardware description language (VHDL) and an FPGA implementation of these units have been successfully performed [28-33].

Finally, the automatic synthesis of fuzzy processors has been discussed in this thesis. The problem of less flexibility in fuzzy processors has been addressed by proposing a novel bit scalable architecture of a fuzzy inference processor. A memory based novel fuzzifier has been designed and developed first time and a novel centre of gravity (COG) based defuzzifier has been designed. A bit scalable fuzzy inference processor using the above mentioned fuzzifier and defuzzifier has also been designed using VHDL and implemented in Vertex FPGA.