

PERFORMANCE EVALUATION OF MULTIPROCESSOR ARCHITECTURES

Author

Manaullah

Supervisor

Prof. M. R. Khan

Deptt. of Electronics &
Comm. Engg. JMI

Co-Supervisor

Prof. Qasim Rafiq

Dept. of Computer Engg.,
AMU

In this millennium research is on to speedup more and more computational power by reducing the size of system. Exploiting parallelism is now a necessity to improve the throughput of computer system. Most of the computer performance improvement so far have been based on technical developments. We have started relying more and more on computer simulation rather than on analysis or experimentation. This has forced the designers to embrace parallel processing and to look for new architectural concepts that have capability of providing orders of magnitude performance increase.

The present work reported in this thesis, is concerned with the development of a new multiprocessor network, called Linearly Extensible Triangle (LED) network. Different existing schemes, for parallel execution of tree structured problems have been implemented on this network. Simulation study have been implemented on this network Simulation study have been carried out to compare the performance of Linearly Extensible Triangle (LED) multiprocessor networks and different dynamic scheduling schemes with other similar multiprocessor networks available in the literature on tree structured types of problem graphs.

The network proposed is a linearly extensible triangle multiprocessor network, which exhibits the desirable properties of similar linearly extensible types of multiprocessor networks. The LED network contain linear extensibility with only single processing element per extension The network has lower diameter, hence reduces the average path length traveled by all messages and contains constant degree per node.

The dynamics scheduling scheme minimum distance scheduling (MDS) and hierarchical balancing method (HBM) available in the literature have been modified and implemented on the proposed network. These scheme forces minimum distance constraint based upon only on the adjacency matrix information of the linearly extensible triangle (LED) network and with relatively small overheads, oversees that the task arrives at proper processor maintaining the task relation even for grossly unbalanced problem graph or in the presence of failing nodes or links. These scheduling schemes are implemented on LED network and other similar multiprocessor networks for tree structured problem to obtain a comparative performance study. HBM and MDS schemes have been tested for performance study on the LED network and his compared with the

other existing similar networks i.e linearly extensible tree (LET), twisted N-Cube, linearly extensible cube (LEC) networks, superiority of the proposed LED network has been established.